

**IN THE CLAIMS**

1-50. Canceled.

26. (New) A semiconductor memory receiving external clock signal comprising:

a dynamic type memory cell array;

a row decoder which receives row address signals and is coupled to row lines in said memory cell array;

a column decoder which receives column address signals and is coupled to column lines in said memory cell array;

a data input latch circuit which its input is coupled to data input node and which its output is coupled to said memory cell array; and

a data output latch circuit which its output is coupled to data output node and which its input is coupled to said memory cell array,

wherein the timing of the data outputted from said data output latch circuit is controlled in response to said external clock signal.

27. (New) The semiconductor memory according to claim 26,

wherein the timing of column address signal inputted and the timing of corresponding data outputted from said data output latch circuit is controlled by a different cycle of said external clock signal.

28. (New) The semiconductor memory according to claim 27, wherein the timing of column address signal inputted is controlled by a first level change of said external clock signal, and

wherein the timing of corresponding data outputted from said data output latch circuit is controlled by a second level change of said external clock signal which occurs after said first level change.

29. (New) The semiconductor memory according to claim 28, wherein the time difference between said first level change and said second level change is one cycle of said external clock signal.

30. (New) The semiconductor memory according to claim 26, wherein the timing of column address signal inputted and the timing of corresponding data outputted from said data output

latch circuit is controlled by a different timing of level change of said external clock signal.

31. (New) The semiconductor memory according to claim 29, further comprising:

an address counter for refresh operation, wherein said semiconductor memory has a page mode.

32. (New) The semiconductor memory according to claim 26, further comprising:

a first latch circuit which receives a external chip select signal and outputs a signal by a timing controlled by said external clock signal; and

a second latch circuit which receives a write enable signal and outputs a signal by a timing controlled by said external clock signal.

33. (New) The semiconductor memory according to claim 32, further comprising:

a row address latch circuit which receives said row address signals from an address terminal and which its output is coupled to said row decoder; and

a column address latch circuit which receives said column address signals from said address terminal and which its output is coupled to said column decoder,

wherein said row and column address latch circuits are controlled by said external clock signal,

wherein said signal outputted from said first latch circuit controls the operation of said row and column address latch circuits, and

wherein said external clock signal has a continuous succession of clock pulses of a constant period.

34. (New) A semiconductor memory chip receiving external clock signal comprising:

a dynamic type memory cell array;

a row decoder which receives row address signals and is coupled to said memory cell array;

a column decoder which receives column address signals and is coupled to said memory cell array;

a data input latch circuit which its input is coupled to data input node and which its output is coupled to said memory cell array; and

a data output latch circuit which its output is coupled to data output node and which its input is coupled to said memory cell array;

wherein the timing of the data outputted from said data output latch circuit is controlled in response to said external clock signal; and

wherein the timing of the data outputted from said data input latch circuit is controlled in response to said external clock signal.

35. (New) The semiconductor memory chip according to claim 34, further comprising:

a row address latch circuit which receives said row address signals from an address terminal and which its output is coupled to said row decoder; and

a column address latch circuit which receives said column address signals from said address terminal and which its output is coupled to said column decoder,

wherein said row and column address latch circuits are controlled by said external clock signal.

36. (New) The semiconductor memory chip according to claim 34,

wherein said semiconductor memory chip has a page mode,  
and

wherein after the consecutive input of different column  
signals are inputted, a precharge operation is set at the end  
of a page mode cycle.

37. (New) The semiconductor memory chip according to  
claim 34, wherein the timing of column address signal inputted  
and the timing of corresponding data outputted from said data  
output latch circuit are each controlled by a different cycle  
of said external clock signal.

38. (New) The semiconductor memory chip according to  
claim 37, wherein the lap between the cycle to control said  
timings is one cycle of said external clock signal.

39. (New) The semiconductor memory chip according to  
claim 34, further comprising a first latch circuit which  
receives a external chip select signal and which controls the  
timing of a output signal by said external clock signal.

40. (New) The semiconductor memory chip according to  
claim 39, further comprising a second latch circuit which

receives a write enable signal and which controls the timing of a output signal by said external clock signal.

41. (New) A semiconductor memory chip receiving external clock signal comprising:

a dynamic type memory cell array;

a row decoder which receives row addresses and is coupled to said dynamic type memory cell array; and

a column decoder which receives column addresses and is coupled to said dynamic type memory cell array,

wherein after a first row address is inputted, a first and second column addresses are inputted consecutively, and

wherein the timing of inputting said first row address, said first and second column addresses are each controlled by a different edge of said external clock signal.

42. (New) The semiconductor memory chip according to claim 41, further comprising:

row address latch circuit which its input is coupled to an address terminal and which its output is coupled to said row decoder; and

a column address latch circuit which its input is coupled to said address terminal and which its output is coupled to said column decoder,

wherein said semiconductor memory has a page mode.

43. (New) The semiconductor memory chip according to claim 42, wherein in a cycle of said page mode there is a precharge time after the consecutive input of first and second column addresses.

44. (New) The semiconductor memory chip according to claim 43, further comprising:

a data input latch circuit which its input is coupled to data input node and which its output is coupled to said memory cell array; and

a data output latch circuit which its output is coupled to data output node and which its input is coupled to said memory cell array,

wherein the time difference between the timing of data outputted from said data output latch circuit and the timing of corresponding column address inputted is controlled by said external clock signal.

45. (New) The semiconductor memory chip according to claim 44, further comprising:

a first latch circuit which receives external chip select signal and outputs a signal by a timing controlled in response to said external clock signal; and

a second latch circuit which receives write enable signal and outputs a signal by a timing controlled in response to said external clock signal.

46. (New) A semiconductor memory receiving external clock signal comprising:

a dynamic type memory cell array;

a row decoder which receives row addresses and is coupled to said dynamic type memory cell array;

a column decoder which receives column addresses and is coupled to said dynamic type memory cell array;

a row address latch circuit which its input is coupled to an address terminal and which its output is coupled to said row decoder; and

a column address latch circuit which its input is coupled to said address terminal and which its output is coupled to said column decoder,

wherein after one row address is inputted to said row address latch circuit, a plurality of column addresses are inputted to said column address latch circuit in series, and wherein the timing of inputting said one row address, said plurality of column addresses are each controlled by said external clock signal.

47. (New) The semiconductor memory according to claim 46, wherein the timing of inputting said one row address, said plurality of column addresses are each controlled by a different rising edge of said external clock signal.

48. (New) The semiconductor memory according to claim 46, wherein the time difference between the timing of each data outputted from said data output latch circuit and the timing of each corresponding column address of said plurality of column addresses inputted is controlled by said external clock signal.

49. (New) The semiconductor memory according to claim 46, further comprising:

a first latch circuit which receives external chip select signal and outputs a signal by a timing controlled by said external clock signal;

a second latch circuit which receives write enable signal and outputs a signal by a timing controlled by said external clock signal;

a data input latch circuit which its input is coupled to data input node and which its output is coupled to said memory cell array; and

a data output latch circuit which its output is coupled to data output terminal and which its input is coupled to said memory cell array,

wherein the timing of the data outputted from said data output latch circuit is controlled by said external clock signal, and

wherein the timing of the data outputted from said data input latch circuit is controlled by said external clock signal.

50. (New) A semiconductor memory chip receiving an external clock signal comprising:

a dynamic type random access memory cell array;

an address input terminal to be supplied with address signals having time multiplexed row address signals and column address signals;

a row address latch having an input which is supplied with said row address signals from said address input terminal;

a column address latch having an input which is supplied with said column address signals from said address input terminal;

a first latch circuit for receiving an external chip select signal in response to said external clock signal;

a second latch circuit for receiving a write enable signal in response to said external clock signal;

a data input latch circuit having an input which is supplied with an external data and an output coupled to said memory cell array;

a data output latch circuit having an input coupled to said memory cell array and an output coupled to said data output node;

a row address decoder having an input which is coupled with an output of said row address latch and an output which is coupled to said dynamic type random access memory cell array;

and a column address decoder having an input which is coupled with an output of said column address latch and an output which is coupled to said dynamic type random access memory cell array,

wherein said row address latch latches said row address signals in response to said external chip select signal latched by said first latch circuit and to a transition edge of said external clock signal,

wherein said column address latch latches said column address signals in response to said external chip select signal latched by said first latch circuit and to a different transition edge of said external clock signal,

wherein said data input and output latch circuits are controlled by said external clock signal.

51. (New) The semiconductor memory according to claim 50, wherein the time difference between said transition edge used for latch operation of said row address latch and said different transition edge used for latch operation of said column address latch is one cycle of said external clock signal.